

**REMARKS**

Claims 1-13 are currently pending in the present application, of which Claim 6 has been amended.

Claim 6 has been amended as suggested by the Examiner. Thus, the claim objection is believed to be overcome.

**Rejection under 35 U.S.C. § 102**

Claims 1-13 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Ferry et al.* (US 6,150,798). Applicant respectfully traverses such rejection insofar as it might apply to the claims as amended herein.

Amended Claim 1 (and similarly Claim 6) now recites a voltage converter having "a first power supply circuit capable of converting an input voltage to an output voltage" and "a second power supply circuit capable of converting said input voltage to said output voltage, wherein said second power supply circuit is connected in parallel with said first power supply circuit."

On page 3 of the Final Office Action, the Examiner asserts that the claimed first and second power supply circuits are disclosed by *Ferry* in Figure 3 as elements 11 and 12, respectively. However, according to *Ferry*, element 11 is for controlling transistors MP and MN in a switched-mode power supply (SMPS) mode, and element 12 is for controlling transistor MP in a linear regulator mode (col. 4, lines 39-42). Thus, elements 11 and 12 are not power supply circuits capable of converting an input voltage to an output voltage, as claimed. Because the claimed invention recites novel features that are not found in *Ferry*, the § 102 rejection is believed to be overcome.

**CONCLUSION**

Claims 1-13 are currently pending in the present application. For the reasons stated above, Applicant believes that independent Claims 1 and 6 along with their respective dependent claims are in condition for allowance.

No fee or extension of time is believed to be necessary; however, in the event that any fee or extension of time is required for the prosecution of this application, please charge it against IBM Deposit Account No. 50-0563.

Respectfully submitted,



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